AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method for optimizing decoupling capacitance in a phase locked loop, comprising:

   inputting a representative power supply waveform having noise to a simulation of the phase locked loop, wherein the representative power supply waveform is obtained from a physical system;

   estimating jitter of the phase locked loop dependent on the inputting;

   adjusting an amount of decoupling capacitance dependent on the estimating; and

   repeating the inputting, estimating, and adjusting until the jitter falls below a selected amount.

2. (Cancelled)

3. (Currently Amended) The method of claim [[2]] 1, wherein the physical system comprises a printed circuit board.

4. (Currently Amended) The method of claim [[2]] 1, wherein the physical system comprises a chip package.

5. (Currently Amended) The method of claim [[2]] 1, wherein the physical system comprises a chip.

6. (Currently Amended) The method of claim 1, wherein the representative power supply waveform is obtained from a location on [[a]] the physical system adjacent to an intended location of the phase locked loop.

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Original) The method of claim 1, wherein the representative power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

11. (Original) The method of claim 1, wherein the simulation of the phase locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

12. (Currently Amended) A computer system for optimizing decoupling capacitance in a phase locked loop, comprising:

a processor;

a memory; and

software instructions stored in the memory adapted to cause the computer system to:

input a representative power supply waveform having noise to a simulation of the phase locked loop, wherein the representative power supply waveform is obtained from a physical system;

estimate jitter of the phase locked loop dependent on the representative power supply waveform having noise;

adjust an amount of decoupling capacitance dependent on the estimate; and

repeat the input, estimate, and adjust until the jitter falls below a selected amount.

13. (Cancelled)

14. (Currently Amended) The computer system of claim [[13]] 12, wherein the physical system comprises a printed circuit board.

15. (Currently Amended) The computer system of claim [[13]] 12, wherein the physical system comprises a chip package.

16. (Currently Amended) The computer system of claim [[13]] 12, wherein the physical system comprises a chip.

17. (Currently Amended) The computer system of claim 12, wherein the representative power supply waveform is obtained from a location on [[a]] the physical system adjacent to an intended location of the phase locked loop.

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Original) The computer system of claim 12, wherein the simulation of the phase locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

23. (Currently Amended) A computer-readable medium having recorded thereon instructions executable by a processor, the instructions adapted to:

input a representative power supply waveform having noise into a simulation of a phase locked loop, wherein the representative power supply waveform is obtained from a physical system;

estimate jitter of the phase locked loop dependent on the representative power supply waveform having noise;

adjust an amount of decoupling capacitance dependent on the estimate; and

repeat the input, estimate, and adjust until the jitter falls below a selected amount.

24. (Cancelled)

25. (Currently Amended) The computer-readable medium of claim [[24]] 23, wherein the physical system comprises a printed circuit board.

26. (Currently Amended) The computer-readable medium of claim [[24]] 23, wherein the physical system comprises a chip package.

27. (Currently Amended) The computer-readable medium of claim [[24]] 23, wherein the physical system comprises a chip.

28. (Currently Amended) The computer-readable medium of claim 23, wherein the representative power supply waveform is obtained from a location on [[a]] the physical system adjacent to an intended location of the phase locked loop.

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Original) The computer-readable medium of claim 23, wherein the representative power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

33. (Original) The computer-readable medium of claim 23, wherein the simulation of the phase locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.